MAS6240E

Piezo Driver with Multi-Mode Charge Pump

- **Both Single Ended and Differential Output**
- **Three-Step Volume Adjusting**
- **Up to 18Vpp Output from 3V and 30Vpp from 5V Supply**
- **One Wire Audio & Shutdown Control**
- **Solution without Inductors**
- **Low External Part Count**
- **MAS6240E2 with 0.125 MHz Switching Frequency for reduced current consumption**

DESCRIPTION

MAS6240 is a piezo driver device that can drive outputs up to 18Vpp from 3V supply and up to 30Vpp from 5V supply. An internal three-mode charge pump generates boosted supply voltage for piezo driver. For adjusting the piezo element sound volume, the charge pump can operate in either of a 1x, 2x or 3x mode. In 1x mode the output voltage is same to the input voltage, in 2x or 3x mode the input voltage is boosted up accordingly 2 or 3 times. Charge pump mode is selected by control pins EN1 and EN2 (see Table 2 on page 3).

MAS6240 is an easy and low-cost solution for piezo driver, since only 4 small value capacitors are needed in addition to sound element - the use of inductors can be avoided. The inductorless design also causes significantly less disturbance to the surrounding circuits making it an ideal choice for sensitive designs.

Control logic is switching the charge pump on at first rising signal of digital input (DIN) pin. The piezo driver is enabled at a second rising edge of a pulse at DIN and the signal is transferred to piezo output VO1. The same signal is inverted into output VO2 for using differential output. The charge pump and piezo driver disable signal will be generated while the signal at DIN has been at low at least for 25ms (typ 16ms). When disabled the piezo driver outputs VO1 and VO2 are pulled to GND.

Continuous logic high level at DIN input causes the charge pump to be turned ON but leaves the piezo driver disabled.

In "disabled" mode (DIN has been low for 15ms typically) all functional blocks are switched off to achieve the quiescent current less than 0.25µA. VOUT voltage still remains near to VIN level.

FEATURES

Piezo Driver & Multi-Mode Charge Pump

- Thin QFN 2x2 and 3x3 12ld packages
- Three-Step Volume Adjusting
- Both Single Ended and Differential Output
- Up to 18Vpp Output from 3V Supply and up to 30Vpp from 5V Supply
- One Wire Audio & Shutdown Control
- Low External Part Count
- Inductorless low EMI solution
- MAS6240E1 is direct replacement for older MAS6240C2 and MAS6240E2 for MAS6240D3

APPLICATIONS

- Piezo Buzzers
- Wrist Watches
- Alarm Clocks
- Handheld GPS devices
- PDAs
- Portable Device with Sound Feature
- White Goods

ABSOLUTE MAXIMUM RATINGS

All voltages with respect to ground.

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	VIN		-0.3	6	V
Outputs and Flying Capacitors Pins Voltages	VOUT		VIN - 0.3	20	V
	CP2, VO1, VO2		-0.3	20	V
	CP1, CN2		-0.3	13	V
Voltage Range for Input Pins	DIN, EN1, EN2, CN1		-0.3	VIN + 0.3	V
Storage Temperature			-55	+150	°C
ESD Rating	V_{HBM}	Human Body Model (HBM) (1)	±1		kV
	V_{CDM}	Charged Device Model (2)	±1		kV

Note: Stresses beyond the values listed may cause a permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.

Note 1: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

All voltages with respect to ground.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Junction Temperature	T_J		-40		+125	°C
Operating Ambient Temperature	T_A		-40	+27	+85	°C
Operating Supply Voltage	V_{IN}		2.2	3.0	5.5	V

ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C, typical values at T_A = 27°C, V_{IN} = 3.0 V, C_1 = 0.1 µF, C_2 = 0.1 µF, C_{OUT} = 0.1 µF, C_{IN} = 1.0 µF, C_{piezo} = 15 nF, digital input DIN=4kHz; unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	VOUT	VOUT pin voltage towards ground at VIN = 3V, load 0…5mA 1x Mode 2x Mode 3x Mode	 2.8 5.2 7.2		 3 6 9	 V
Shutdown Current	I_{SD}	DIN = 0V, **Note 1**		7	250	nA
Internal Switching Frequency (Charge Pump)	F_{OSC}	MAS6240E1 MAS6240E2	0.7 87	1 125	1.4 175	MHz kHz
Current Consumption	I_{CC}	Charge Pump (no load): MAS6240E1 1x Mode 2x Mode 3x Mode MAS6240E2 1x Mode 2x Mode 3x Mode		 55 340 640 55 160 250	 100 700 1400 100 300 700	 µA
		Single ended application (C_{piezo} = 15nF; f=4kHz): MAS6240E1 1x Mode 2x Mode 3x Mode MAS6240E2 1x Mode 2x Mode 3x Mode		 0.25 1.15 2.44 0.25 0.95 2.05		 mA
		Differential application (C_{piezo} = 15nF; f=4kHz): MAS6240E1 1x Mode 2x Mode 3x Mode MAS6240E2 1x Mode 2x Mode 3x Mode		 0.8 3.5 7.6 0.8 3.3 7.3		 mA
Signal Frequency	F_{AUDIO}		0.2	4	8	kHz
VOUT Turn-ON Time (From DIN signal HIGH to 90% VOUT steady state)	t_{ON}	2x Mode 3x Mode		30 60	200 300	µs
Shut Down delay	t_{OFF}	Time before device shutdown after DIN signal goes to LOW	11	16	23	ms
Control Input Threshold	V_{IH} V_{IL}	EN1, EN2, DIN pins	1.6		 0.55	V V
Control Input Current	I_{IH} I_{IL}	V_{DIN} = 3V, (900kΩ pull down) V_{DIN} = 0V		3.4 0	7 1	µA µA
	 I_{IH} I_{IL}	V_{DIN} = 3V $V_{EN1,EN2}$ = 3V, (900kΩ pull down) $V_{EN1,EN2}$ = 0V		 3.4 0	 7 1	 µA µA
	 I_{IH} I_{IL}	V_{DIN} = 0V, **Note 2** $V_{EN1,EN2}$ = 3V $V_{EN1,EN2}$ = 0V		 0 0	 1 1	 µA µA

Note 1: DIN has been low at least 25 ms.
Note 2: EN1 and EN2 pins are at high-Z state while V_{DIN}=0V.

BLOCK AND APPLICATION DIAGRAM

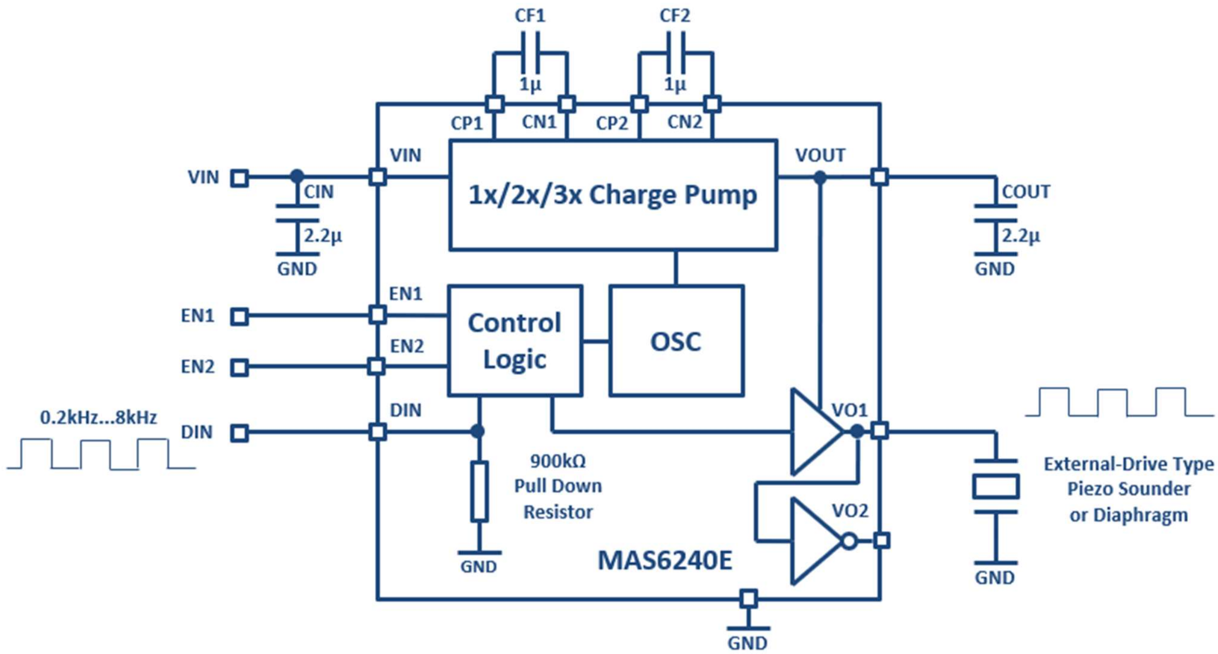


Figure 1. Charge Pump + Single End Piezo Driver (max 9Vpp @ VIN=3V)

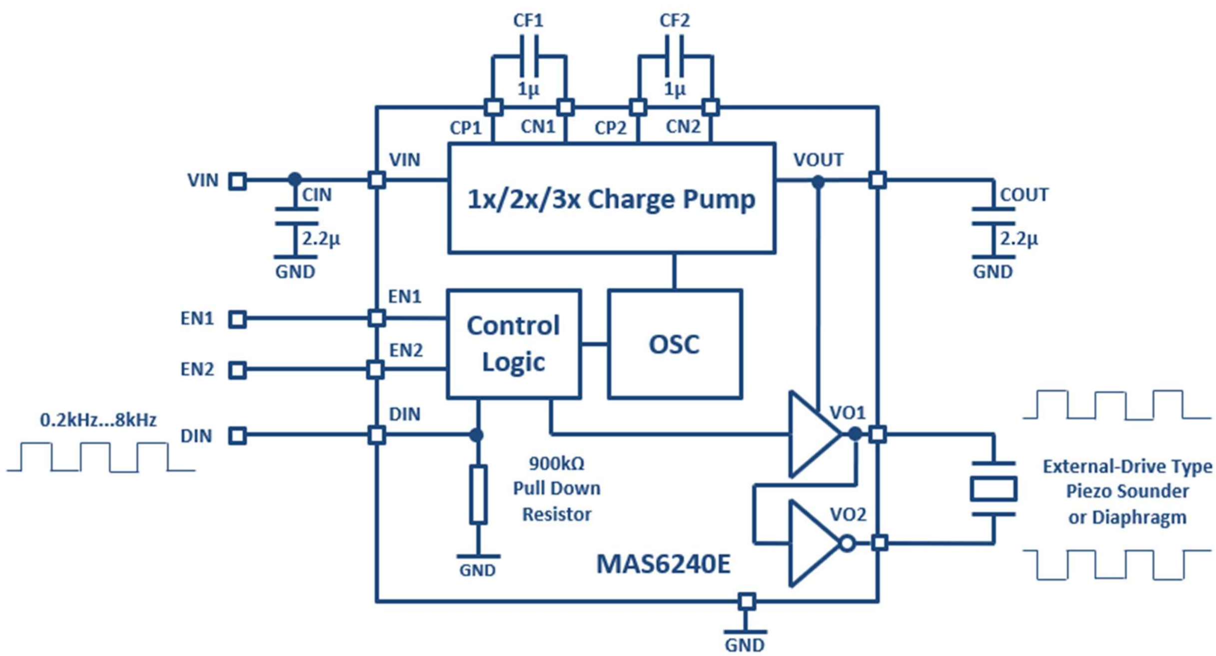


Figure 2. Charge Pump + Differential Piezo Driver (max 18Vpp @ VIN=3V)

The input (CIN), flying (CF1, CF2) and output (COUT) capacitor value selections affect output ripple and inrush current drawn from input during start-up. See table 1 for selecting capacitor values at different applications. The lowest inrush current can be achieved at the configuration 3 when using additional 10Ω series resistor between supply voltage and VIN. All capacitors must be ceramic type with low ESR and meeting following minimum voltage ratings: min 6.3V for CIN and CF1-CF2 and min 16V for COUT (20V for 5.5V supply).

Table 1. Capacitor value selection configurations at different applications

Config.	CIN	CF1-2	COUT	Application
1	0.1µF	0.1µF	0.1µF	Minimum size layout (only MAS6240E1 recommended)
2	1µF	1µF	1µF	Small size layout
3	2.2µF	1µF	2.2µF	Low output ripple application
4	10µF	1µF	2.2µF	Coin cell operated device with low input & output ripple (MAS6240E2 recommended)

The voltage ripple at VOUT output is approximately proportional to ratio of piezo load capacitance and charge pump output capacitor (COUT). Thus, the output ripple can be reduced by choosing COUT which is much larger relative to piezo capacitance value. However, the COUT should not be chosen too large since it lengthens output voltage rise time and increases inrush current drawn from input. For low inrush current the CIN should be made much larger than the COUT.

Table 2 presents charge pump boosting modes selected by control pins EN1 and EN2.

Table 2. Charge Pump boosting mode selection

DIN	EN1	EN2	Charge Pump (VOUT voltage)
0	-	-	OFF (~VIN)
1	0	0	OFF (~VIN)
1	0	1	1x Mode (VIN)
1	1	0	2x Mode (2xVIN)
1	1	1	3x Mode (3xVIN)

Note: In above table pulsed signal at digital input DIN is taken as “1” if pulse low time is less than 5 ms!

APPLICATION INFORMATION – EXTERNAL PROTECTION

When a mechanical or thermal shock is applied to the piezo sounder it can produce high surge voltage which may cause permanent damage to the IC. If in your application the device is expected to face such shocks, it is recommended to use external protection against this surge voltage.

External protection can be based either on Zener diodes or an external resistor (~1kΩ…2kΩ). See figures 3 and 4 illustrating Zener and resistor protection circuits in both differential and single-ended piezo driving configurations. The Zener diode protection is suited for applications requiring the highest sound pressure level (SPL) since it does not reduce achievable SPL. The resistor protection solution has the lowest cost but it has impact on SPL especially in case of piezo with a large capacitance.

When using Zener diode protection, the Zener voltage should be chosen high enough to not limit selected output voltage (VOUT) level but also not being too far away to provide the best protection. In case driving piezo sounder in 3x mode at maximum 3.3 supply voltage the output can be VOUT=9.9V a suitable choice for a nominal Zener voltage is for example 11V when taking account Zener voltage tolerances.

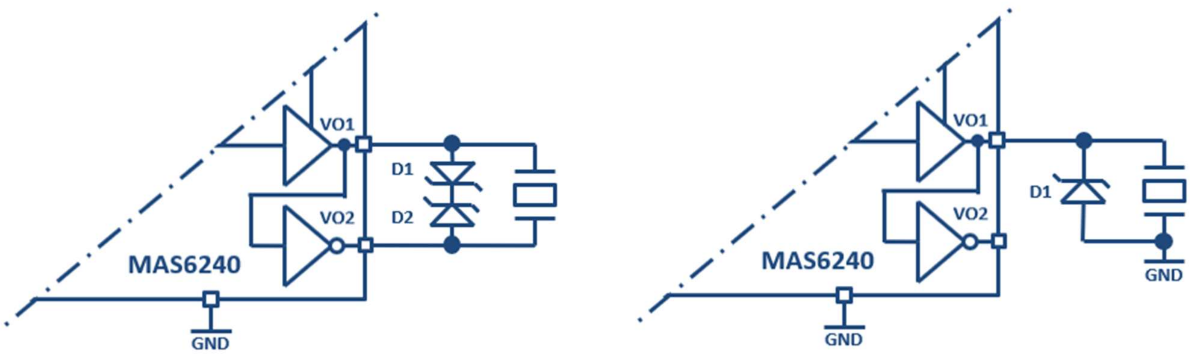


Figure 3. External Zener diode protection of piezo driver outputs

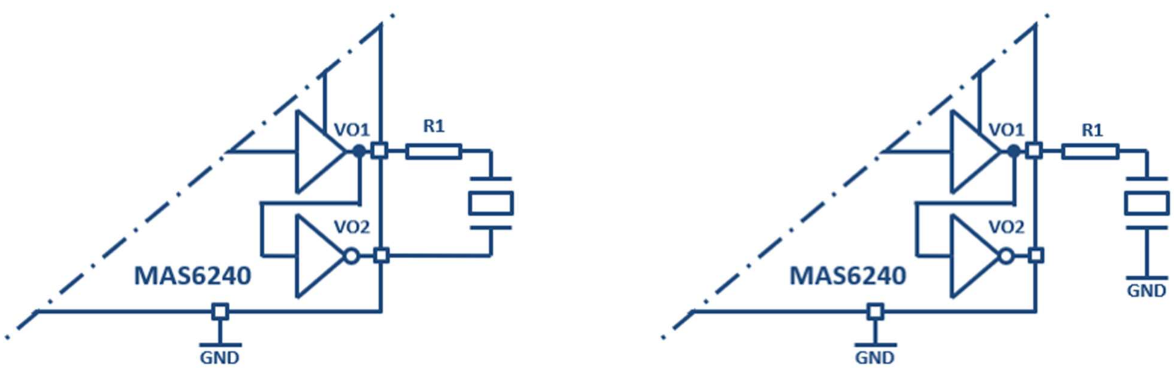


Figure 4. External resistor protection of piezo driver outputs

DETAILED DESCRIPTION

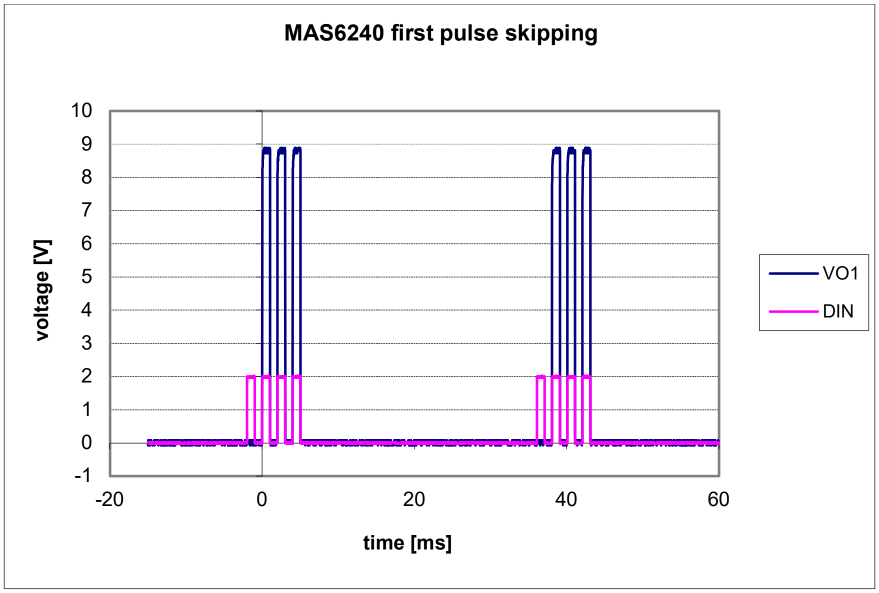


Figure 5. Enabling output VO1

The piezo driver is enabled at the second rising edge of the signal at DIN, thus the signal is transferred to the piezo output VO1. An inverted output VO2 is enabled at the same time, but it is optional to take it in use. Control logic is switching the charge pump on at first rising signal of digital input DIN pin. If only one rising edge is fed to the input DIN, the piezo driver remains disabled. The VO1 and VO2 outputs are at GND when the piezo driver is disabled.

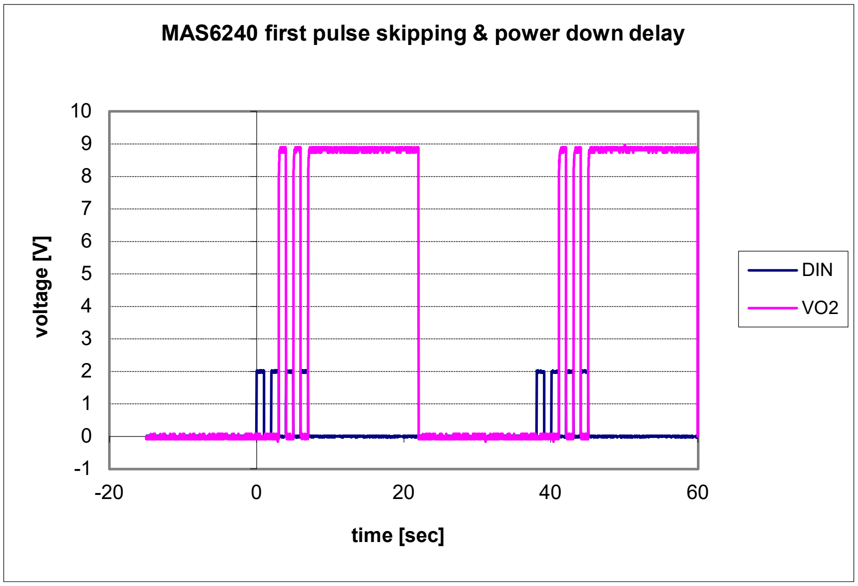
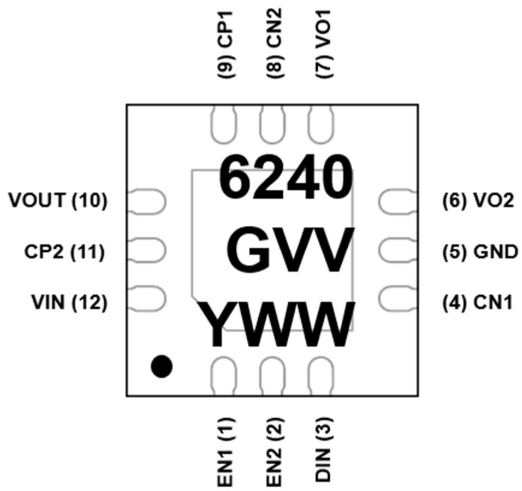


Figure 6. Disabling VO2

Figure 6 shows VO2 signal. The charge pump and piezo driver disable signal will be generated after the signal at DIN has been low at least for 25 ms. In the figure 6 the switch-off delay is about 16 ms. Again when new pulses are fed into DIN, the charge pump and piezo driver will be enabled.

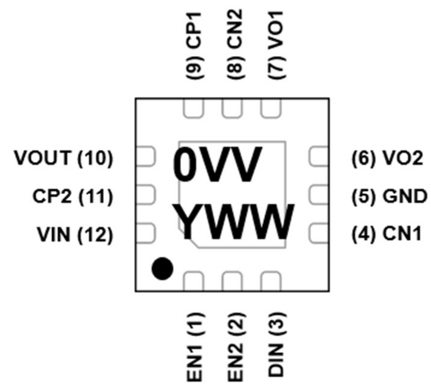
DEVICE OUTLINE CONFIGURATION

QFN-12 3x3



Top Marking Information:
6240 = Product Number
G = Lead Free, RoHS
VV = Version (E1, E2)
Y = Year (1 = 2021 etc.)
WW = Week

QFN-12 2x2



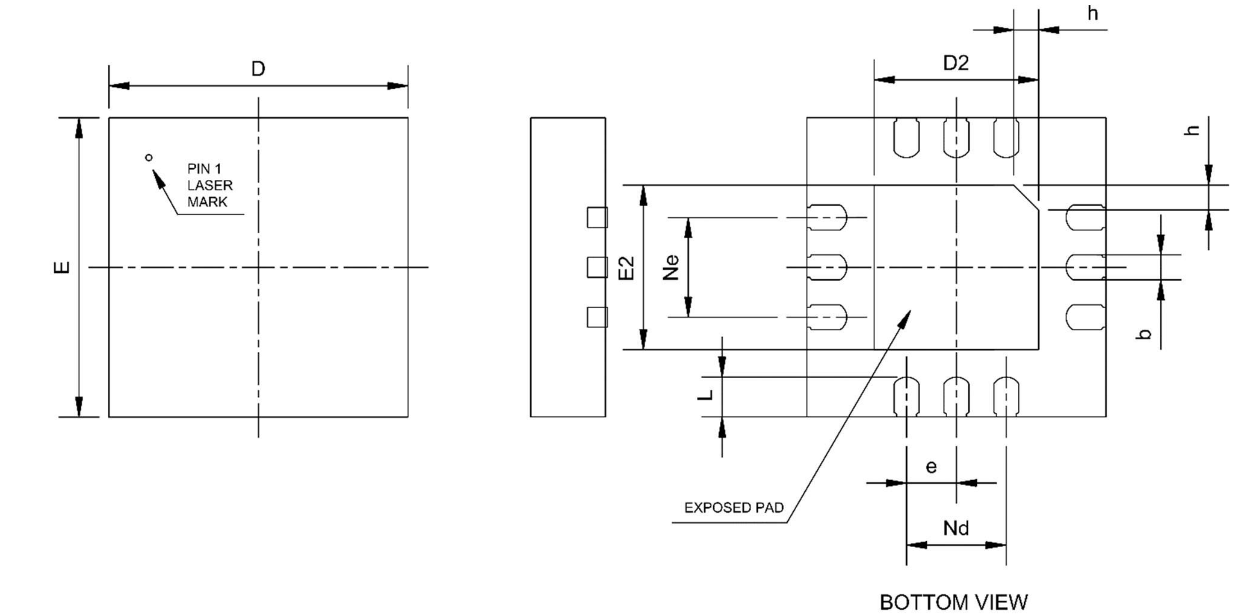
Top Marking Information:
0 = Product Number
VV = Version (E1, E2)
Y = Year (1 = 2021 etc.)
WW = Week

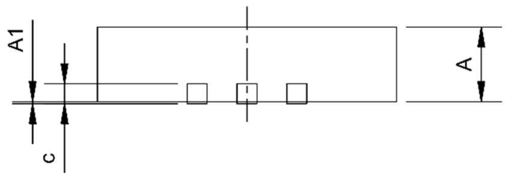
QFN-12 2x2x0.5, QFN-12 3x3x0.75 PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
EN1	1	DI	Charge pump mode selection input 1	
EN2	2	DI	Charge pump mode selection input 2	
DIN	3	DI	Enable signal + Digital signal input	
CN1	4	AI/O	Flying capacitor 1 negative terminal	
GND	5	G	Supply ground	
VO2	6	DO	Digital audio signal output 2	
VO1	7	DO	Digital audio signal output 1	
CN2	8	AI/O	Flying capacitor 2 negative terminal	
CP1	9	AI/O	Flying capacitor 1 positive terminal	
VOUT	10	AO	Charge pump output	
CP2	11	AI/O	Flying capacitor 2 positive terminal	
VIN	12	P	Power supply	
EXP_PAD	-	P	Exposed pad connected to GND	1

G = Ground, P = Power, D = Digital, A = Analog, I = Input, O = Output
Note1: On PCB the exposed can be either connected to GND or left floating.

PACKAGE (QFN-12 2x2x0.5) OUTLINE



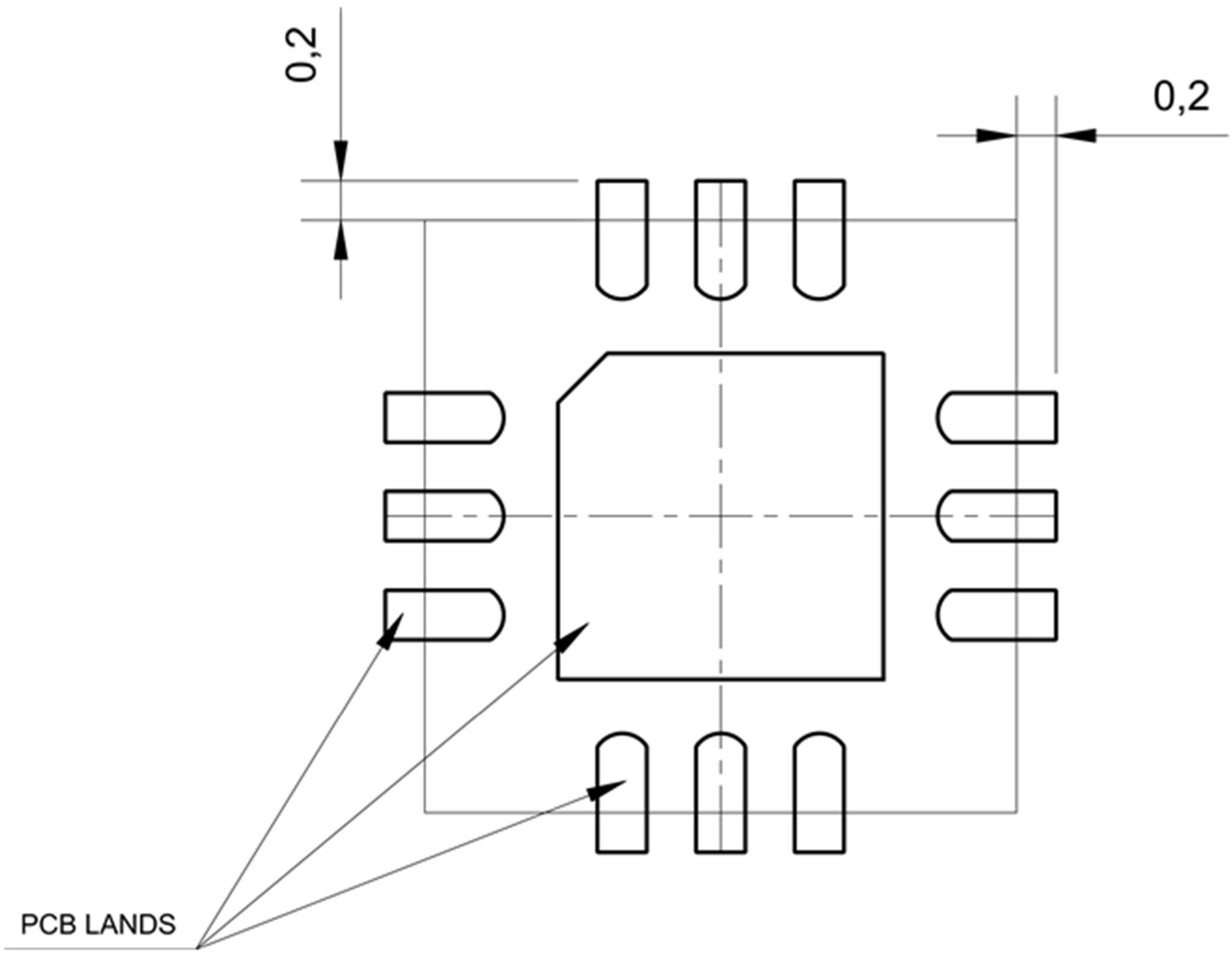


Note: Package drawing is only referential but table dimensions are accurate.

Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.45	0.5	0.55	mm
A1	0	0.02	0.05	mm
b	0.15	0.20	0.25	mm
c	0.10	0.15	0.20	mm
D	1.90	2.00	2.10	mm
D2 (Exposed.pad)	1.00	1.10	1.20	mm
e	0.40 BSC			mm
Ne	0.80 BSC			mm
Nd	0.80 BSC			mm
E	1.90	2.00	2.10	mm
E2 (Exposed.pad)	1.00	1.10	1.20	mm
L	0.15	0.20	0.25	mm
h	0.15	0.20	0.25	mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.

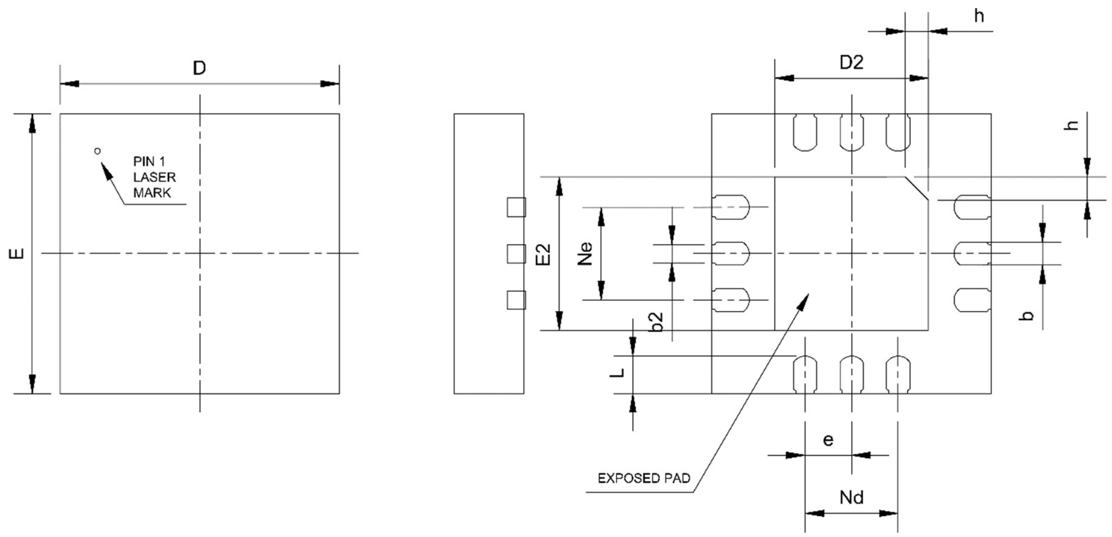
QFN-12 2x2x0.5 PCB LAND PATTERN

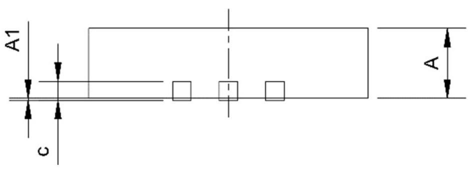


Notes

- I/O lands should be 0.2mm longer than QFN pads and extend the same 0.2mm outside package outline
- exposed pad land size should be the same as QFN exposed pad size
- solder resist opening should be 120μm…150μm larger than the land size resulting in 60μm…75μm clearance between copper land and solder resist

PACKAGE (QFN-12 3x3x0.75) OUTLINE



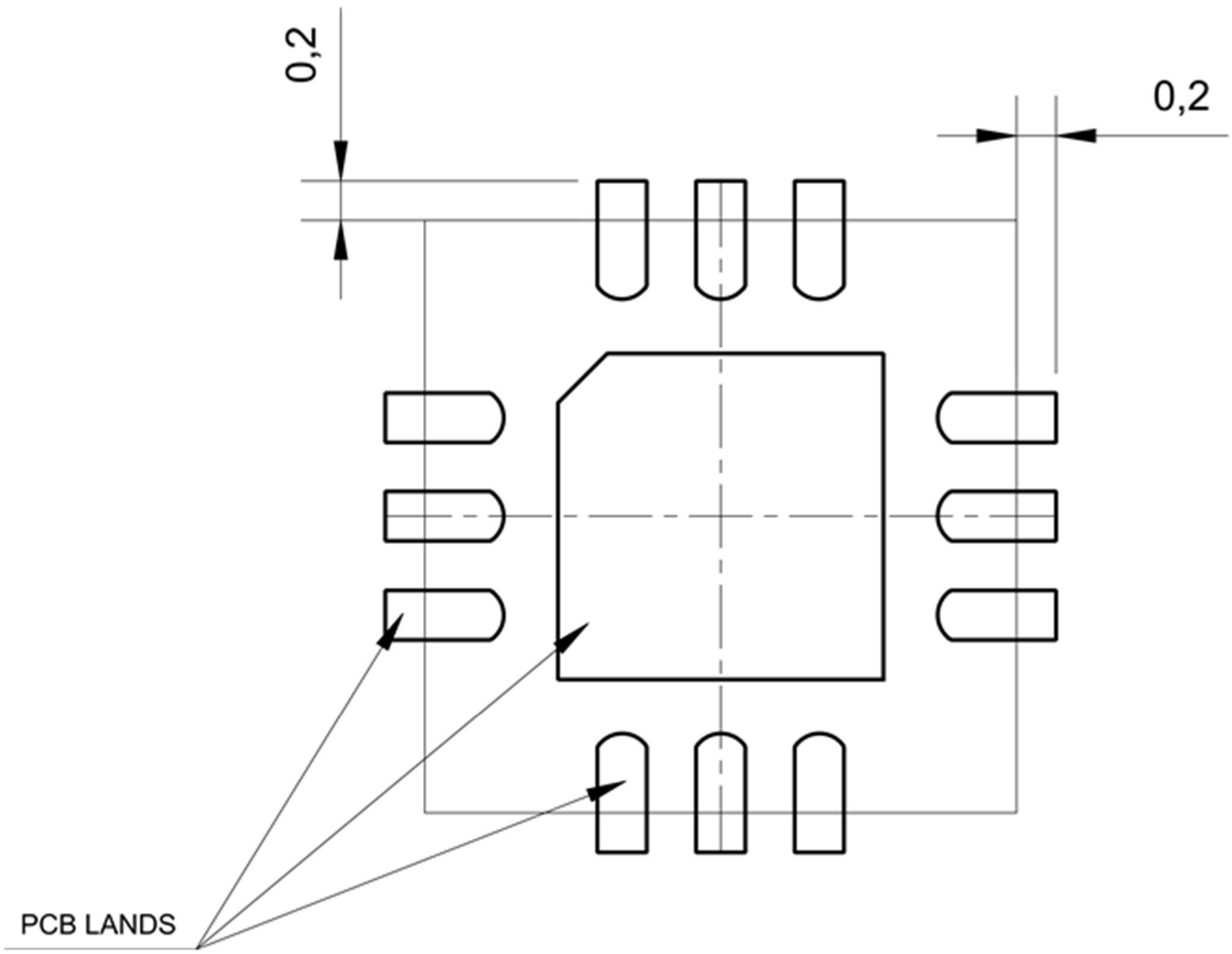


Note: Package drawing is only referential but table dimensions are accurate.

Symbol	Min	Nom	Max	Unit
PACKAGE DIMENSIONS				
A	0.70	0.75	0.80	mm
A1	---	0.02	0.05	mm
b	0.20	0.25	0.30	mm
b2	0.15	0.20	0.25	mm
c	0.18	0.20	0.25	mm
D	2.90	3.00	3.10	mm
D2 (Exposed.pad)	1.55	1.65	1.75	mm
e		0.50 BSC		mm
Ne		1.00 BSC		mm
Nd		1.00 BSC		mm
E	2.90	3.00	3.10	mm
E2 (Exposed.pad)	1.55	1.65	1.75	mm
L	0.35	0.40	0.45	mm
h	0.20	0.25	0.30	mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.

QFN-12 3x3x0.75 PCB LAND PATTERN



Notes

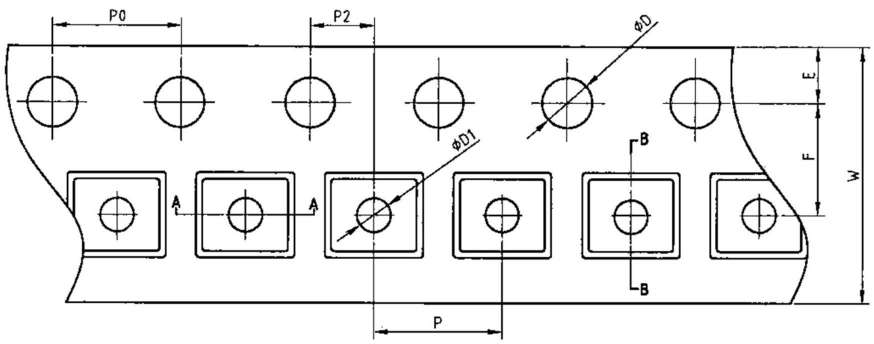
- I/O lands should be 0.2mm longer than QFN pads and extend the same 0.2mm outside package outline
- exposed pad land size should be the same as QFN exposed pad size
- solder resist opening should be 120µm…150µm larger than the land size resulting in 60µm…75µm clearance between copper land and solder resist

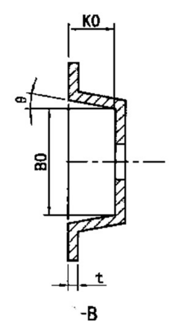
SOLDERING INFORMATION

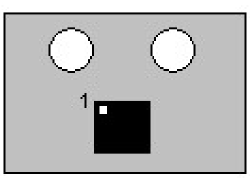
◆ **For Lead-Free / Green QFN 2mm x 2mm x 0.5mm and 3mm x 3mm x 0.75mm**

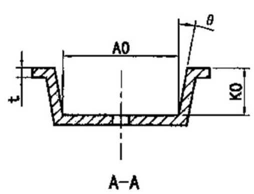
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Lead Finish	7.62 - 25.4 µm, Matte Tin
Moisture Sensitivity Level (MSL)	1 (per J-STD-020)

QFN 2x2x0.5 EMBOSSED TAPE SPECIFICATIONS









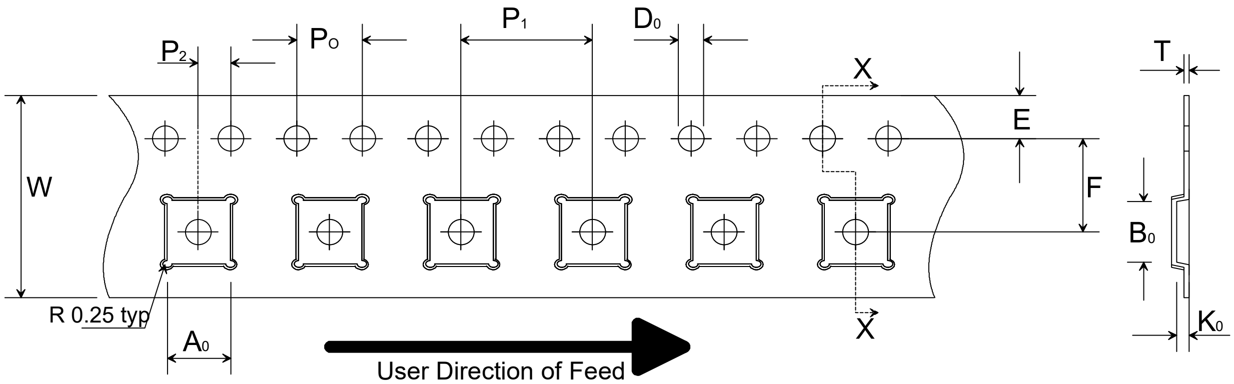
User Direction of Feed

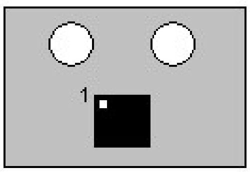
Orientation on tape

Dimension	Min/Max	Unit
A0	2.13 ±0.05	mm
B0	2.13 ±0.05	mm
D	1.50 ±0.1	mm
D_1	1.00 +0.25/-0.00	mm
E	1.75 ±0.10	mm
F	3.50 ±0.05	mm
K0	0.88 ±0.05	mm
P	4.00 ±0.10	mm
P0	4.00 ±0.10	mm
10P0	40.00 ±0.20	mm
P_2	2.00 ±0.05	mm
t	0.254 ±0.02	mm
W	8.00 +0.3/-0.1	mm
θ	5 MAX	°

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative

QFN 3x3x0.75 EMBOSSED TAPE SPECIFICATIONS





Orientation on tape

Dimension	Min/Max	Unit
A_o	3.30 ±0.10	mm
B_o	3.30 ±0.10	mm
D_o	1.50 +0.1/-0.0	mm
E	1.75	mm
F	5.50 ±0.05	mm
K_o	1.10 ±0.10	mm
P_o	4.0	mm
P_1	8.0 ±0.10	mm
P_2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 ±0.3	mm

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS6240E1Q2106 MAS6240E2Q2106	Piezo Driver	QFN 2x2x0.5 12 lead, REACH & RoHS Compliant	Ø7” Tape and Reel 3000 pcs / r
MAS6240E1Q1306 MAS6240E2Q1306	Piezo Driver	QFN 3x3x0.75 12 lead, REACH & RoHS Compliant	Ø13” Tape and Reel 5000 pcs / r
MAS6240E1Q1309 MAS6240E2Q1309	Piezo Driver	QFN 3x3x0.75 12 lead, REACH & RoHS Compliant	Tape 500 pcs
MAS6240E1WA300 MAS6240E2WA300	Piezo Driver	EWS Tested 8” wafers, thickness 406 µm ± 5%	
MAS6240E1WA305 MAS6240E2WA305	Piezo Driver	Dies in waffle pack, thickness 406 µm ± 5%	

◆ **The formation of product code**

An example for MAS6240E1Q1306:

MAS6240	E1	Q13	06
Product name	Product Version: E1: F_{OSC} = 1 MHz E2: F_{OSC} = 0.125 MHz	Package: Q13 = QFN 3 x 3 x 0.75 Q21 = QFN 2 x 2 x 0.5 WA3 = 406 µm thick EWS tested wafer	Delivery format: 00 = Tested Wafer 05 = Tested Dies 06 = Tape and Reel 09 = Tape

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